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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/678,417	**Applicant(s)** FAN ET AL.	
	Examiner Michael Trinh	**Art Unit** 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 07 July 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 12 and 14-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 12 and 14-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment and RCE filed on July 07, 2006. Claims 12 and 14-19 are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Bond et al (5,991,156).

Bond et al teach (at Figs 3-4; col 5, lines 1-49; and Figs 1A-2B; col 3, line 30 through col 4) a method for fabricating an integrated circuit package comprising at least the steps of: providing a substrate having opposite first and second surfaces and conductive traces 22,17 extending there between (Figs 1A-1B; col 3, lines 39-57), the substrate having a cavity therein; fixing a heat sink slug 34 (Fig 3, col 5, lines 1-15) in form of a substantially flat plate to the first surface of the substrate 36/16 (Figs 3,1A) such that the heat slug 34 spans the opening cavity; mounting a semiconductor die 32/12 to said heat slug 34, said semiconductor die 32 being disposed in said cavity; wire bonding 38 said semiconductor die 34 to ones of the conductive traces at the second surface of the substrate (Figs 3-4, col 5, lines 16-23; Fig 1B); encapsulating said wire bonds 38 and said semiconductor die 32 in an encapsulating material 40 (Fig 4; col 5, lines 12-23); and forming a ball grid array on a first surface of said substrate such that bumps 24 of said ball grid array are in electrical connection with ones of said conductive traces 17/22 (Figs 3-4; col 5, lines 24-49; Figs 1A-1B; cols 3-4), wherein the heat slug 34 is fixed to said first surface of said substrate on which the ball grid array is formed; and wherein, as shown in Figures 3-4, the substrate 36 is substantially the same thickness as the semiconductor die 32.

Claim Rejections - 35 USC § 103

2. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins, III (5,583,377) taken with Suzuki (6,028,358) and Wagner et al (5,309,322).

Higgins teaches (at Figs 1-8; cols 2-8) a method for fabricating an integrated circuit package comprising at least the steps of: providing a substrate having opposite first and second surfaces and conductive traces 18,14 extending there between, the substrate having a cavity therein; fixing a heat sink slug in form of a plate (e.g. 66/68 in Fig 3) to the first surface of the substrate 62 such that the heat slug spans 66/68 the opening cavity 20 (e.g. Figs 3, col 5, lines 44 through col 6; col 2, line 50 through col 3, line 42), wherein the base portion of heat sink slug preferably extends below circuitized substrate; however, the base portion can be planar with the circuitized substrate (col 6, lines 60-68; lines 7-68; col 8,lines 49-51); mounting a semiconductor die 13 to said heat slug 66, at least a portion of said semiconductor die 13 being disposed in said cavity 20; wire bonding 19 said semiconductor die 13 to ones of the conductive traces 14/18 at the second surface of the substrate 62 (Figs 3,2,1, col 3, line 11 through col 5); encapsulating said wire bonds 19 and said semiconductor die 13 in an encapsulating material 33 (col 4, lines 35-42), and forming a ball grid array 21 on a first surface of said substrate 62 such that bumps 21 of said ball grid array are in electrical connection with ones of said conductive traces 14 (col 3, lines 30-42), wherein fixing the heat slug is fixed to said substrate comprises fixing said heat slug 66/68 to said first surface of said substrate 62 (Fig 3; col 5, lines 44-67; col 2, lines 50 through col 3, line 42; col 4); and wherein, as shown in Figure 3, the substrate 62 is about the same thickness as the semiconductor die 13, with the semiconductor die 13 to be planar with the surface of the substrate 62 (Figure 3; and col 8, lines 14-20 and 50-56; and col 6, lines 41-67).

Higgins already teaches spanning the opening cavity 20 with a heating slug in the form of a plate having the base portion of heat plug preferably extending below circuitized substrate; however, the base portion can be planarized with the circuitized substrate (col 6, lines 60-68; 7-68; and col 8,lines 49-51).

Higgins thus lacks showing the heat slug in the form of a substantially flat plate, wherein substrate is substantially the same thickness as the semiconductor die.

However, Suzuki teaches and shows at Figure 1A (first embodiment, col 3, line 55 through col 4) spanning the opening cavity with a heating slug 4 in the form of a plate having the base portion of heat sink plug extending below circuitized substrate, and also teaches and show at Figure 3 (second embodiment; col 5, lines 39-55; Figs 7-8; col 6, line 45 through col 7; Fig 9, col 7, lines 15-24) spanning the opening cavity with a heating slug 13 in the form of a substantially flat plate. In Higgins, as shown in Figure 3, the substrate 62 is about the same thickness as the semiconductor die 13, with the semiconductor die 13 to be planar with the surface of the substrate 62 (Figure 3; and col 8, lines 14-20 and 50-56; and col 6, lines 41-67).

Wagner further teaches providing the substrate 24 is substantially the same thickness as the semiconductor die 26 (col 3, lines 55-63; Fig 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fixing the heat slug in the form of the plate of Higgins to the substrate by alternatively employing the heat slug in the form of a substantially flat plate as shown and prima facie taught by Suzuki, wherein Suzuki prima facie teaches forming a heating slug 13 in the form of a substantially flat plate (see Figure 3) instead of using the heat slug 4 having sidewalls and flanges as shown in Figure 1A of Suzuki. This is because these heat slugs are alternative and art recognized equivalent for substitution, wherein a semiconductor device package having the flat heat slug is planar, and wherein a plurality of semiconductor device packages having the flat heat slugs can be effectively stacked together so as to form stacked devices. Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the semiconductor device of Higgins by making the substrate to have substantially the same thickness of the semiconductor die, as further taught by Wagner. This is because of the desirability to minimize the length of bonding wires, and because of the desirability to form the semiconductor integrated circuit package having a substantially planar surface and structure.

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins, III (5,583,377), Suzuki (6,028,358), and Wagner et al (5,309,322), as applied to claim 12, and further of Jamieson et al (6,060,777).

Higgins, Suzuki and Wagner teach (at Figs 1-8; cols 2-8) a method for fabricating an integrated circuit package as applied to claim 12 above.

Higgins teaches fixing the heat slug 66/68 to the substrate by adhesive, but lacks fixing by a solder reflow technique.

However, Jamieson et al teach (at Figs 2-4; col 2, lines 37-61) fixing a heat slug 30 of metal to a board substrate 32 by solder reflowing technique or adhesive.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fixing the heat slug of Higgins to the substrate by employing a solder reflowing technique as taught by Jamieson, because soldering and adhesive fixing techniques are alternative and art recognized equivalent techniques for substitution in fixing the metal heat slug to the substrate so that the heat slug can be firmly and strongly attached to the substrate in a reliable manner.

4. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins, III (5,583,377), Suzuki (6,028,358), and Wagner (5,309,322), as applied to claim 12, and further of Li (5,982,621).

Higgins, Suzuki, and Wagner teach (at Figs 1-8; cols 2-8) a method for fabricating an integrated circuit package as applied to claim 12 above.

Prior to encapsulating, Higgins lacks mounting a die adapter to the semiconductor die (as recited in claims 15-16), mounting a heat spreader to the substrate (as recited in claims 17-18), and mounting a heat spreader such that at least one side wall of the heat spreader is mounted to the substrate and a top portion of the heat spreader contacts the adapter (as recited in claim 19).

However, prior to encapsulating of an encapsulating material 40, Li teaches (at Figs 4-6,2; col 2, line 31 through col 3, line 7): Re claim 15, mounting a die adapter 20 to a semiconductor die 31; Re claim 16, wherein encapsulating comprises encapsulating the wire bonds 32 and the semiconductor die 31 and surrounding the die adapter 20 such that a surface of said die adapter 20 is exposed (Figs 4-6; col 2, lines 31 through col 2, line 7); Re claims 17-18, mounting a heat spreader 10 to the substrate 30 (Figs 4,1-2; col 2, lines 12-31; abstract); and Re claim 19, mounting a heat spreader, prior to encapsulating, such that at least one side wall of said heal spreader 10 is mounted to said substrate 30 and a top portion of said heat spreader contacts said die adapter 20.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the integrated circuit package of the references including Higgins by, prior to encapsulating, mounting the die adapter to the semiconductor die and the heat spreader to the substrate such that at least one side wall of said heal spreader is mounted to the substrate and a top portion of the heat spreader contacts the die adapter, as taught by Li. This is because of the desirability to quickly cool the die during operation by dissipating the heat from the chip through the die adapter and the heat spreader, thereby improving the reliability and working efficiency of the integrated circuit package.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bond et al (5,991,156), as applied to claim 12, taken with Jamieson et al (6,060,777).

Bond et al teach (at Figs 3-4; col 5, lines 1-49; and Figs 1A-2B; col 3, line 30 through col 4) a method for fabricating an integrated circuit package as applied to claim 12 above.

Bond teaches fixing the heat slug 32 to the substrate 36 by adhesive, but lacks fixing by a solder reflow technique.

However, Jamieson et al teach (at Figs 2-4; col 2, lines 37-61) fixing a heat slug 30 of metal to a board substrate 32 by solder reflowing technique or adhesive.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fixing the heat slug of Bond to the substrate by employing a solder reflowing technique as taught by Jamieson, because soldering and adhesive fixing techniques are alternative and art recognized equivalent techniques for substitution in fixing the metal heat slug to the substrate so that the heat slug can be firmly and strongly attached to the substrate in a reliable manner.

6. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bond et al (5,991,156), as applied to claim 12, in view of Li (5,982,621).

Bond et al teach (at Figs 3-4; col 5, lines 1-49; and Figs 1A-2B; col 3, line 30 through col 4) a method for fabricating an integrated circuit package as applied to claim 12 above.

Prior to encapsulating, Bond et al lack mounting a die adapter to the semiconductor die (as recited in claims 15-16); mounting a heat spreader to the substrate (as recited in claims 17-18); and mounting a heat spreader such that at least one side wall of the heat spreader is mounted to the substrate and a top portion of the heat spreader contacts the adapter (as in claim 19).

However, prior to encapsulating of an encapsulating material 40, Li teaches (at Figs 4-6,2; col 2, line 31 through col 3, line 7): Re claim 15, mounting a die adapter 20 to a semiconductor die 31; Re claim 16, wherein encapsulating comprises encapsulating the wire bonds 32 and the semiconductor die 31 and surrounding the die adapter 20 such that a surface of said die adapter 20 is exposed (Figs 4-6; col 2, lines 31 through col 2, line 7); Re claims 17-18, mounting a heat spreader 10 to the substrate 30 (Figs 4,1-2; col 2, lines 12-31; abstract); and Re claim 19, mounting a heat spreader, prior to encapsulating, such that at least one side wall of said heal spreader 10 is mounted to said substrate 30 and a top portion of said heat spreader contacts said die adapter 20.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the integrated circuit package of Bond by, prior to encapsulating, mounting the die adapter to the semiconductor die and the heat spreader to the substrate such that at least one side wall of said heal spreader is mounted to the substrate and a top portion of the heat spreader contacts the die adapter, as taught by Li. This is because of the desirability to quickly cool the die during operation by dissipating the heat from the chip through the die adapter and the heat spreader, thereby improving the reliability and working efficiency of the integrated circuit package.

Response to Arguments

*** Applicant's remarks filed July 07, 2006 have been fully considered but they are not persuasive, and in moot of new ground of rejections.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
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Michael Trinh
Primary Examiner